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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) :	Dureseti CHIDAMBARRAO	Group Art Unit: 2813
Appln. No. :	10/715,400	Examiner: J. M. Mitchell
Filed :	November 19, 2003	Confirmation No.: 5307
For :	SILICON DEVICE ON Si:C-OI AND SGOI AND METHOD OF MANUFACTURE	

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

DECLARATION UNDER 37 C.F.R. §1.131

Sir:

We, Dureseti CHIDAMBARRAO, Omer H. DOKUMACI, and Oleg G. O.G. GLUSCHENKOV, do hereby declare:

1. We are co-inventors of the subject matter disclosed and recited in independent claims 1 and 27 of the above-identified application.

2. We completed the invention of claims 1 and 27 (and those claims dependent thereon) in the United States before November 13, 2003, as evidenced below.

CONCEPTION

3. Before November 13, 2003 we conceived a method of manufacturing a structure comprising the steps of: forming shallow trench isolation (STI) in a substrate; providing a first material on the substrate; providing a second material, which is different

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than the first material, on the substrate; mixing the first material and the second material into the substrate by a thermal anneal process to form a first island and second island at a nFET region and a pFET region, respectively; and forming a layer of material on the first island and the second island having a lattice constant different than the first island and the second island, wherein the STI relaxes and facilitates the relaxation of the first island and the second island.

4. Before November 13, 2003, we also conceived a method of manufacturing a semiconductor structure, comprising the steps of: forming a substrate; forming shallow trench isolation of high temperature stable amorphous material in the substrate; thermally annealing at least one material into the substrate to form a first island and a second island of mixed material; and growing an Si layer on at least the first island, straining the Si layer in one of a compressive and tensile stress, wherein the material is at least one of a first material and a second, different material.

5. Evidence of such conceptions as disclosed and recited in claims 1 and 27 of the application is shown in an embodiment of which is evidenced by IBM Invention Disclosure FIS8- -0323 (hereinafter referred to as "the Invention Disclosure") attached hereto as Exhibit A. The Invention Disclosure attached hereto is a photocopy of and are identical to the originals, except that the pertinent dates have been removed therefrom.

6. All relevant dates removed from the Invention Disclosure and other documents attached hereto are before November 13, 2003.

7. The benefits and features of the recited invention are shown and described in the Invention Disclosure and accompanying documents.

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8. These features and others are exemplified in the figures accompanying the Invention Disclosure.

DUE DILIGENCE

9. At least inventor Dureseti Chidambarrao communicated with outside patent counsel, Andrew M. Calderon, in preparing a patent application based on the Invention Disclosure.

10. We worked diligently on the preparation of the patent application by first submitting the Invention Disclosure to in-house IBM counsel. The Invention Disclosure was forwarded to Mr. Calderon, on July 11, 2003. We worked diligently with Mr. Calderon, until final draft patent application was completed to our satisfaction. Communications took place between at least one of the Inventors and Mr. Calderon at least between October 16, 2003, and November 6, 2003.

11. A final draft of the patent application and formal documents were forwarded to the Inventors. The formal documents were executed on November 12, 2003. The application and formal documents were filed in the USPTO on November 19, 2003.

12. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section

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1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dureseti Chidambarrao — Date

Omer H. Dokumaci — Date

Oleg G. Gluschenkov — 5/8/2006 — Date

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